The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GARY L. SWOBODA and ROBERT A. MCGOWAN

Appeal 2007-1754
Application 09/943,599[1]
Technology Center 2100

Decided: August 29, 2007

Before KENNETH W. HAIRSTON, JOHN C. MARTIN, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1, 4, 5, 13, 15, 16, 23, 24, and 27-30. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

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[1] This application is a divisional of Application Ser. No. 09/798,561, filed Mar. 2, 2001, now U.S. Pat. 6,985,848.

STATEMENT OF THE CASE

Appellants invented a system and method for providing data processor emulation information including providing a trace stream used to monitor activity such as program flow and memory accesses. In one embodiment, trace information is provided including identifying a program counter value that corresponds to a particular data processing operation. The counter value is expressed as an offset that indicates a number of program counter values in the program counter trace stream by which the corresponding program counter value is offset from the synchronization marker in the program counter trace stream.[2] Claim 1 is illustrative with the disputed limitations italicized for emphasis:

1. A method of providing data processor emulation information, comprising:

providing a program counter trace stream of program counter values used by a data processor;

inserting a synchronization marker into the program counter trace stream; and

providing trace information indicative of each data processing operation performed by the data processor, including identifying a program counter value that corresponds to the data processing operation, said identifying step including *expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.*

The Examiner relies on the following prior art references to show unpatentability:

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[2] *See generally* Specification at 8:8-11 and 30:18-31:1.

Sites	US 5,764,885	Jun. 9, 1998
Mann	US 6,009,270	Dec. 28, 1999
Edwards	US 6,732,307 B1	May 4, 2004 (filed Oct. 1, 1999)

1. Claims 1, 4, and 5[3] stand rejected under 35 U.S.C. § 102(e) as being anticipated by Mann.
2. Claims 13, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sites in view of Mann.
3. Claims 23, 24, and 27-30 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sites in view of Mann and further in view of Edwards.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer[4] for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

OPINION

The Anticipation Rejection

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[3] Although the Examiner indicates that claims 1-10 and 12 are rejected under 35 U.S.C. § 102(e) (Answer 4), claims 2, 3, and 6-10 (among other claims) have been cancelled. *See* Answer 2; *see also* Br. 3.

[4] An Examiner's Answer was first mailed in May 3, 2006, but was revised on Dec. 5, 2006 following an Order from the Board. A third Examiner's Answer was mailed Mar. 13, 2007. We refer to the March 2007 Answer throughout this opinion.

We first consider the Examiner's rejection of claims 1, 4, and 5 under 35 U.S.C. § 102(e) as being anticipated by Mann. Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983).

The Examiner has indicated how the claimed invention is deemed to be fully met by the disclosure of Mann (Answer 4-6). Regarding independent claim 1, Appellants argue that Mann fails to identify a program counter value and express this program counter value as an offset which indicates the number of program counter values in the program counter trace stream by which the corresponding program counter value is offset from the synchronization marker in the program counter trace stream as claimed (Br. 11). Appellants emphasize that the operation of synchronization marker "TSYNC"[5] fails to anticipate the claimed synchronization marker since, among other things, the trace address values following such a marker are not offset from the synchronization marker value. Rather, the trace address values are offset from the prior and unchanged segment base address (Br. 13-15).

[5] "TSYNC" is a synchronization register that allows injection of synchronizing address information (Mann, col. 16, ll. 3-5). *See also* p. 7, *infra*, of this opinion.

The Examiner contends that Mann teaches a synchronization marker in the form of Trace Codes ("TCODES") in the trace stream where all TCODEs (except TCODE=0001) are synchronization events (Answer 15). The Examiner further contends that TCODE # 0001 provides the subsequent offset information as 15 one bit results for subsequent branching outcomes offset from the base address (Answer 16). The Examiner adds that Mann's TYSNC register is loaded into a counter that counts down and causes insertion of the synchronization marker (i.e., the TCODES) with the base program counter address (Answer 19).

We will not sustain the Examiner's rejection of independent claim 1. Mann discloses a processor that provides trace synchronization information. A key feature in Mann's system is ensuring that program address information is provided in trace records with sufficient frequency. To this end, the processor determines whether each trace record includes address information. Based on this determination, a counter counts each record that lacks address information.[6] When the count of such trace records lacking address information reaches a predetermined number, the current program address is provided as a trace entry. As a result, the system ensures that synchronizing address information is provided periodically even for records that lack such address information (Mann, Abstract; col. 3, ll. 8-30).

In Mann, an instruction trace record is 20-bits wide and comprises two primary fields: (1) TCODE (Trace Code)[7], and (2) TDATA (Trace Data).

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[6] Mann indicates that such trace records lacking address information include conditional branch instructions. These trace records only indicate whether the branch was taken (Mann, col. 2, l. 66 – col. 3, l. 5; col. 15, ll. 61-66).
[7] Eleven different TCODES can be reported. *See* Table 6 (Mann, col. 13, ll. 28-49).

Conditional branch events (i.e., events lacking address information) are reported with such a format using TCODE=0001 and the TDATA field containing 1-bit branch outcome trace entries. As each new conditional branch is encountered, a new 1-bit entry is added on the left and any other entries shifted to the right by one bit (Mann, col. 14, ll. 7-16; Fig. 6A).

We disagree with the Examiner's assertion that these conditional branch results provide the claimed offset and will decide the subsequent number of counter values to be added to the base address (Answer 16-17). Mann's bit-shifting technique (to the extent that such bit-shifting can be considered as program counter values) uniquely identifies 15 different conditional branch events for reporting purposes; it is not used as an offset with respect to the base address. That is, the TDATA field of a TCODE=0001 entry merely indicates that *a conditional branch was taken.*

When a branch target address must be reported, the conditional branch TDATA field is then marked as complete. The target address is then recorded in a trace entry pair, with (1) the first entry (TCODE=0010) providing the high 16-bits of the target address, and (2) the second entry (TCODE=0111) providing the low 16-bits of the target address (Mann, col. 14, ll. 25-34; Fig. 6B).

Simply put, the TDATA field for conditional branch events (TCODE=0001) merely indicates a *status* (i.e., whether a conditional branch was taken). Once the conditional branch TDATA field is marked as complete, this conditional branch status indication (using TCODE=0001) is likewise completed. Nothing in the reference expressly or inherently teaches that this status indication data forms any part of, or constitutes an offset with respect to, the reported *address* (i.e., the 32-bit data reported as a trace entry

pair) – the result of an independent process utilizing TCODES 0010 and 0111.

Nor do we find Mann's counter functionality as anticipating independent claim 1. As we indicated previously, Mann's counter counts each trace record that lacks address information (i.e., records with TCODE=0001). The counter is initially loaded to a value contained in the TSYNC register. For each trace entry having address information, the counter is reloaded with this TSYNC register value. However, for each trace record that lacks address information, the counter is decremented by one. If the counter reaches zero, a trace entry is automatically provided that includes the current program address (e.g., the most recent retired instruction) along with TCODE=0110 (Trace Synchronization) (Mann, col. 16, ll. 3-55; Fig. 7).

Although each occurrence of trace records without address information (e.g., conditional branches) results in a counter value that is "offset" with respect to the TSYNC register value, such an offset does not correspond to an offset *from the synchronization marker,* as claimed. The inserted program address (i.e., having a TCODE=0110) is unaffected by this offset. Rather, such an offset merely dictates *when* to provide a trace entry with current address information.

For the foregoing reasons, we find that Miller does not disclose all limitations of independent claim 1. Accordingly, we will not sustain the Examiner's rejection of that claim or dependent claims 4 and 5.

The Obviousness Rejections

We likewise cannot sustain the Examiner's obviousness rejections under 35 U.S.C. § 103 of (1) independent claim 13 based on the combined disclosures of Sites and Mann, and (2) independent claims 23 and 24 based on the combined disclosures of Sites, Mann, and Edwards for similar reasons.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966).

Discussing the question of obviousness of a patent that claims a combination of known elements, the Court in *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740, 82 USPQ2d 1395, 1396 (2007) explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.*, 425 U.S. 273, 189 USPQ 449 (1976)] and *Anderson's-Black Rock*[*, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 163 USPQ 673 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740, 82 USPQ2d at 1396. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.* at 1740-41, 82 USPQ2d at 1396. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 1741, 82 USPQ2d at 1396 (quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Independent claims 13, 23, and 24 call for, in pertinent part, a program counter identifier operable for expressing a corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which the corresponding program counter value is offset from the synchronization marker in the program counter trace stream. Our previous discussion regarding the shortcomings of Mann regarding this limitation applies equally here and we

incorporate that discussion by reference.[8] Moreover, neither Sites nor Edwards teaches or suggests this feature.

Since neither Sites nor Edwards cures the deficiencies of Mann regarding the offset limitation noted above, the Examiner has not established a prima facie case of obviousness for independent claims 13, 23, and 24. Accordingly, we will not sustain the Examiner's rejection of those claims or dependent claims 15, 16, and 27-30.

DECISION

We have not sustained the Examiner's rejections with respect to all claims on appeal. Therefore, the Examiner's decision rejecting claims 1, 4, 5, 13, 15, 16, 23, 24, and 27-30 is reversed.

REVERSED

tdl/ce

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[8] *See* pp. 5-7, *supra*, of this opinion.